REMARKS

Claims 1 - 8 remain pending in the present application. No amendments were made by the present response. Reconsideration of the claims is respectfully requested in view of the following discussion.

Rejections Under 35 U.S.C. §102

Claims 5 - 8 were rejected under 35 U.S.C. §102 over **Kioke** (EP 0953963). It is submitted that nothing in the cited prior art teaches or suggests all the features in the present claimed invention. For instance, nothing in the cited prior art teaches or suggests the claimed means for stopping (claims 5 and 7) and circuit for stopping (claims 6 and 8). As recited in these claims, the means/circuit for stopping stops the frequency adjustment operation based on the number of sampling clocks found in the field, when it is judged that the width of the region where the input video exists is smaller than the number of horizontal effective pixels.

As described in the Background section of the present specification, unique characteristics associated with horizontal RAMP image are addressed. For instance, a horizontal RAMP image has no sharp edge for specifying a horizontal video start position or a horizontal video end position, and is easily affected by noise or jitter components. When the horizontal ramp image is inputted, therefore, the number of horizontal effective pixels cannot be accurately detected. As a result, accurate clock automatic adjustment cannot be performed (*see e.g.*, page 9 of the present specification).

The present invention (*see, e.g.*, the second embodiment) overcomes such problems so that when a horizontal RAMP image is inputted, the display region narrow video detection circuit 87 detects the inputted video as a narrow video, so that the clock adjustment operation is stopped (*see e.g.*, page 54). In addition, the clock phase detection circuit 89 can identify the most suitable delay amount in order to detect the best point of the phase of clocks on the basis of the change in the difference between the horizontal video start count value and the horizontal video end count value. Such features for changing the amount of the delay is recited in the phase adjustment means/circuit in claims 7 and 8. With such features, it is possible to judge that the input video is switched to the narrow video and stop the automatic adjustment operation of the frequency of the sampling clocks or the phase of the sampling clocks. Accordingly, the automatic adjustment operation of the sampling clocks is not erroneously preformed, and the most stable phase relationship is kept between pixel data representing the video signal and the sampling clocks, thus making possible a display of stable video on a pixel corresponding panel (*see e.g.*, pages 60 - 61 of the present specification).

In contrast, **Kioke** does not teach or suggest the claimed means/circuit for stopping, nor the phase adjustment means/circuit. With regard to the means/circuit for stopping, the Office Action referred to column 13, lines 19 - 31 of **Kioke**. However, the cited portion of **Kioke** merely describes the behavior of the H counter 152 (*see e.g.*, Figure 4). This is similar to the description of the H counter 82 of the present application (*see e.g.*, Figure 7), and does not anticipate the claimed means/circuit for stopping, nor the phase adjustment means/circuit.

As for the present claimed phase adjustment means/circuit, the Office Action cited column 11, line 58 to column 12, line 4 of **Kioke** regarding this feature. However, the mere disclosure for a delay circuit 161 in **Kioke** does not at all correspond to the behavior of the phase adjustment means/circuit recited in claims 7 and 8. There is no teaching or suggestion in **Kioke** for changing the amount of the delay according to the specific conditions recited in the phase adjustment means/circuit in claims 7 and 8. For at least the reasons discussed above, the present claimed invention of claims 5 to 8 patentably distinguish over the prior art.

Rejections Under 35 U.S.C. §103

Claims 1-4 were rejected under 35 U.S.C. §103 over **Kioke**, in view of **Haruhiko** (JP 07264440). It is submitted that nothing in the prior art, either alone or in combination teaches or suggests all of the features recited in the present claimed invention of claims 1-4.

The Office Action stated that "**Kioke** fails to disclose a threshold value control means for controlling a second threshold value depending on the level of the video data outputted from the analog to digital converter ..." The Office Action made the further reference to **Haruhiko** for allegedly disclosing a circuit that automatically generates a threshold level in response to a received video signal, and comparing threshold level with the video signal (referring to the Abstract of **Haruhiko**). However, even if **Kioke** were to be combined with **Haruhiko**, for the sake of argument, the present claimed invention is still not achieved.

Independent claims 1 and 3 recite a threshold value control means that changes the value of the second threshold value, depending on the level of the video data outputted from the analog to digital converter. This feature, viewed in combination with other claimed features, overcomes problems in the prior art.

As described on pages 40-41 of the present specification, the conventional sampling clock adjustment circuit relies on set threshold values for start position judgment and end position judgment (*see e.g.*, Figure 5). In a case where the input video signal is a signal having a low luminance, the threshold values are set to small values. Accordingly, the horizontal video effective periods L1 and L2 actually detected are significantly longer than a theoretical value L in the horizontal video effective period. That is, the detection precision of the number of horizontal effective dots is lowered. Even if the detection precision of the number of horizontal effective dots is lowered, an adjustment unit at the time of fine phase adjustment must be fine in order to generate sampling clocks having as suitable a frequency as possible, with respect to the input video signal, so that a time period required for the fine adjustment is lengthened.

In contrast, the sampling clock adjustment circuit according to the present claimed invention can change the threshold value for end position judgment depending on the level of the input video signal, as shown in Figure 4. Accordingly, the threshold value for end position judgment need not be set in conformity in the case where the input video signal is a signal having a low luminance. Instead, it can be set to a large value. As a result, the horizontal video effective periods L1 and L2 actually detected can have values close to the theoretical value L in the horizontal video effective

period. This also means that the necessity for fine phase adjustment is reduced, and the adjustment unit at the time of fine phase adjustment can be reduced, making it possible to improve the adjustment precision as well as shortening the adjustment time.

Nothing in **Kioke** or in the further reference to **Haruhiko** addresses such claimed features. Indeed, **Haruhiko** ***teaches away*** from the present claimed invention because its sets a threshold level in conformity with the received video signal. This creates the similar problems as described by way of Figure 5 of the present application regarding the conventional problems. For at least these reasons, the present claimed invention of claims 1-4 patentably distinguish over the prior art.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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